IN THE CLAIMS

1 - 13. (*Canceled*)

14. (*Currently Amended*) A method for forming a semiconductor device with reduced Miller capacitance comprising the steps of:

heavily doping a substrate with a first conductivity dopant to form a drain region;

growing an epitaxial layer on the substrate and lightly doping the epitaxial layer with a dopant of the first conductivity;

implanting the surface of the epitaxial layer with dopants of a second polarity opposite in polarity to the first conductivity dopant;

covering the substrate with a trench mask having openings corresponding to desired trench regions and removing material from the exposed regions to form trenches;

growing an oxide layer **of a substantially constant thickness** on the trench walls and floor and diffusing the second conductivity dopant to form well regions adjacent the trench sidewalls;

~~in said trench regions~~ forming **over said oxide layer on said trench walls and floor** upper and lower conductive layers and separating the layers with a first dielectric layer; **and** forming source regions in the surface of the epitaxial layer with dopant of the first conductivity.

15. (*Original*) The method of claim 14 comprising the further step of covering the wafer with a source metal region.

16. (*Original*) The method of claim 14 comprising the further step of connecting the source metal regions to the lower conductive trench layers at locations proximate the periphery of the semiconductor device.

17. (*Original*) The method of claim 14 wherein the dopant of the first conductivity is p-type and the dopant of the second conductivity is n-type.

18. (*Original*) The method of claim 14 wherein the dopant of the first conductivity is n-type and the dopant of the second conductivity is p-type.

19. (*Currently Amended*) The method of claim 14 wherein the bottom of the upper conductive layer is approximately on the same level as the bottom of the ~~of the third layer~~ **well regions** of second conductivity.

20. (*Original*) The method of claim 14 wherein the dielectric layer separating the two conductive layers is silicon nitride.

21. (*Original*) The method of claim 14 further comprising the step of adding a second interlevel dielectric layer above said upper conductive layer.

22. (*Currently Amended*) The method of claim 21 wherein said second interlevel dielectric layer ~~isborophosphosilicate~~ **is borophosphosilicate** glass.